Communication interfaces

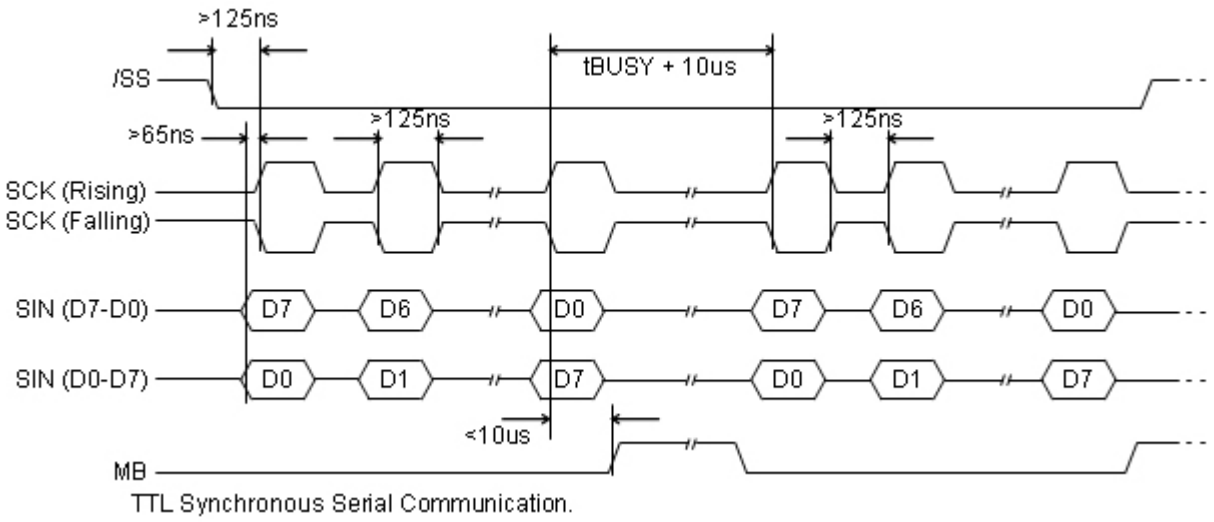
The following table lists many popular interfaces used by host systems with their key attributes.
A common 0V ground connection is required between host and module except for USB and RS485.

interface	type	key signal connections	cable	bit rate	character	graphic
synchronous serial	Clock Serial	Clock, Sin, Reset, (C/D)	< 1.3m	<1MHz	**AU, CUx-T2 / V**	**GU-8, -K6xx**
	SPI	Clock, Sin, Sout, /SS, Reset	< 2m	< 1MHz	**CUx-V**	**-K6xx**
	I²C	Clock, Bi Directional Data	< 1m	< 1MHz	**Custom**	**Custom**
asynchronous serial	TTL / CMOS	SIN, SOUT	< 1m	< 250kHz	**CUx-T, -V**	**-K610, 3000**
	RS232C>	RXD, TXD, DTR, CTS	< 30m	< 115kHz	**CUx-V**	**-K612, 3000**
	RS485	A, B	< 1000m	< 115kHz	**Custom**	**-K611**
	USB	A, B	< 2m	< 2MHz	**Custom**	**GU-3x01**
parallel	M68 BUS	E, R/W, Rs, D0-D7	< 0.5m	< 32MHz	**CUx-U**	**GU-3xx / 8xx**
	i80 BUS	/WR, /RD, A0, D0-D7	< 0.5m	< 32MHz	**CUx-U**	**GU-3xx / 8xx**
	PORT	STROBE, BUSY, D0-D7	< 2m	< 8MHz	**CUx-T**	**Custom**

Synchronous serial interfaces

A clock signal output by the host system provides a synchronizing reference for communicating data bits on a separate data input/output. The data should be stable on either rising edge or falling edge of the clock waveform depending on the system protocol. Since synchronous communication can easily be corrupted by noise, a reset signal is used prior to critical events to ensure both host and module are coordinated.

A 'clock serial' interface is the simplest method with single direction 'send' data to module. An additional signal line C/D may be used for command and data register selection.
The SPI interface is similar to clock serial, except a 'receive' data line 'Sout' and a device select line '/SS' can be used to select the module. The I²C interface uses a bi-directional data line and a software address protocol to select a module.



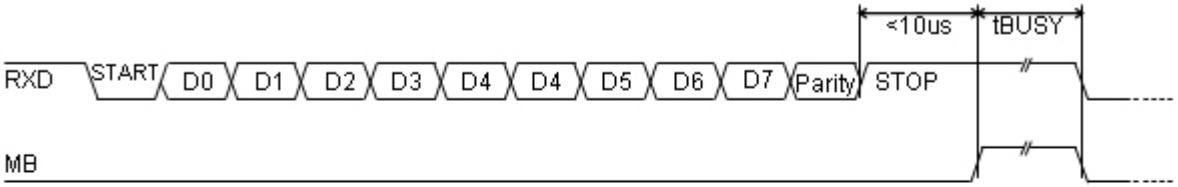
TTL Synchronous Serial Communication.

Asynchronous serial interfaces

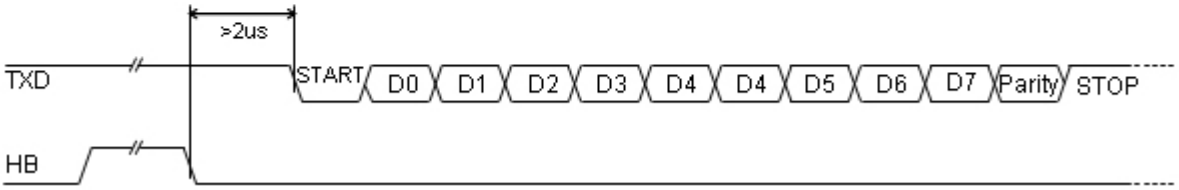
Communication is achieved by initiating a change of state in the data signal (start bit) followed by 8 fixed frequency periods (baud rate) for the synchronized transmission of data. This enables a 2 wire solution for many applications with inherent re-synchronization after each 8 bit data byte.

Transmission between host and module can be made at CMOS/TTL logic voltage levels over distances up to 0.5 meter. The idle state is logic high with data rates up to 115K bits per second.
Greater distance is achieved using RS232 voltage levels (+/-12volts) or a differential system like RS485 which uses two signal wires where the logic level is dependent on the polarity of the wires.

After each data byte, a period is required to allow the module time to process the received data. A hardware control line can be used to indicate to the host that the module is busy. In certain modules an XOFF (13H) character is transmitted to the host to indicate the receive buffer is full. When ready, the module sends the character XON (11H).



TTL Asynchronous serial communications from host system to VFD module

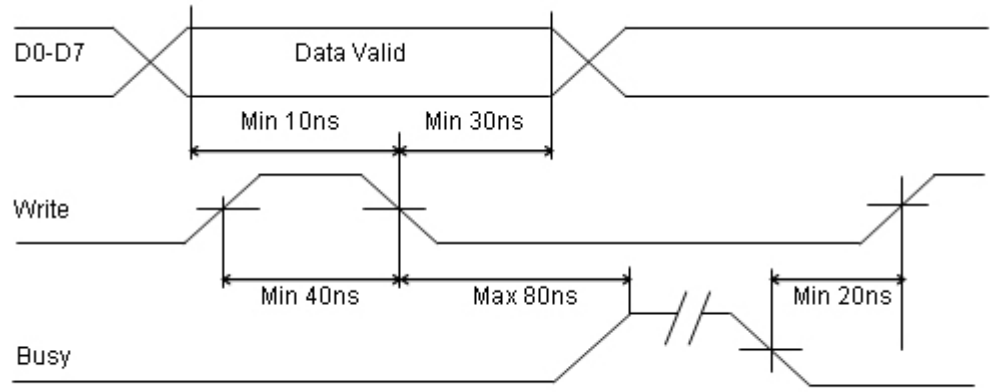


TTL Asynchronous serial communications from VFD module to host system

Parallel interfaces

The conventional CPU distributed data method uses a parallel 8 bit data bus. Two bus configurations evolved to provide data transfer control which are known as M68 bus and i80 bus.
The M68 bus has an (E)nable clock signal and a direction control signal (R/W).
The i80 bus has a separate (/WR) signal for controlling the sending of data and (/RD) for receiving data.
Many modules allow either data bus to be connected by configuring a jumper link on the module PCB.
Additionally, one of the CPU address lines (A0 through to A15) can be used to select different data registers inside the module via the Rs, C/D or A0 input. This allows many additional display functions to be performed with a single command byte.

When several peripheral devices connect to the same data and control bus, a chip select signal (/CS or CS)



Parallel Communication

Other interfaces

Wireless, Ethernet and Optical interfaces have evolved for messaging applications. Interface modules are available in the market to convert these interfaces to RS232.

power on reset

When power is applied to the display module, an internal reset circuit ensures the internal micro-controller or ASIC initializes correctly. The host system should allow at least 100ms before sending data to the module.

hardware reset

Modules with a hardware reset allow the host system to restart the initialization sequence to ensure system integrity. The specification will define the period which should be allowed before data is transmitted.